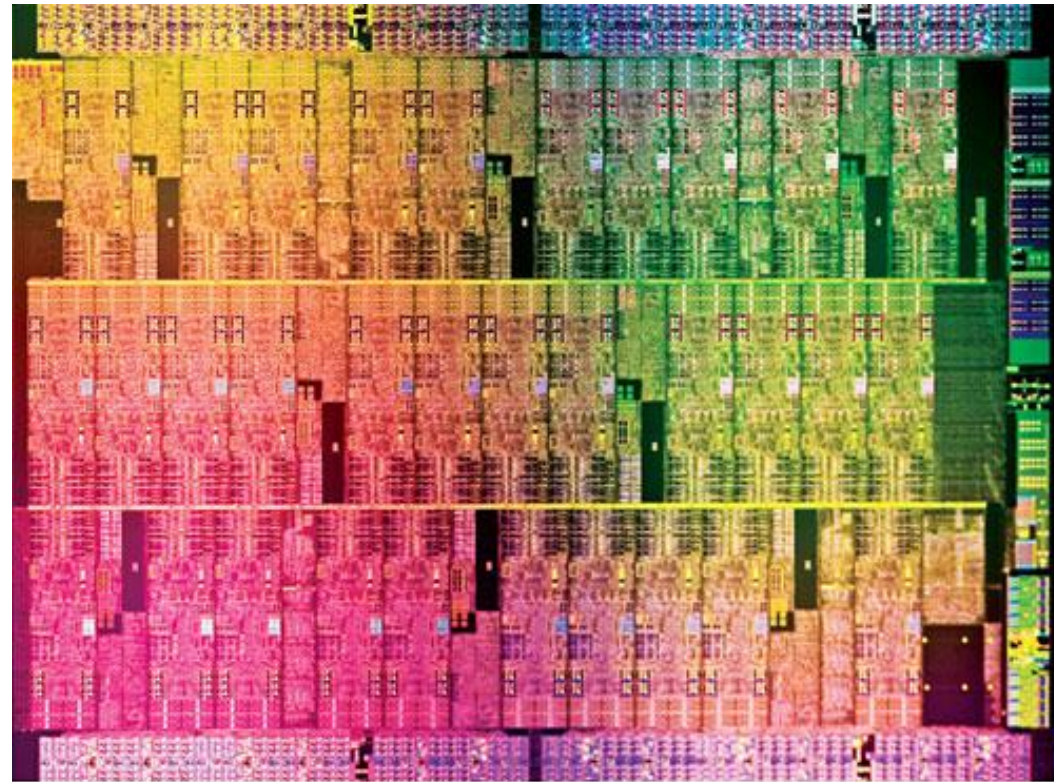


Welcome to ChE 384T/323

- **Chemical Engineering for Micro/Nano Fabrication**



Intel 22nm chip technology

Grant Willson

<http://willson.cm.utexas.edu>



Course Information

- Please read the syllabus carefully
- Class web site is <http://willson.cm.utexas.edu>
- Lecture notes and announcements will be posted on our site
- This is a lecture Course...
 - Please ask questions.....many questions!
 - Make every effort to attend each lecture and presentation
 - There is no text but there will be reading assignments
- Undergrad course (323) vs Grad Course (384T)
 - Oral Presentation for grad students.
 - Undergrads and Graduates will be graded separately
- Periodic Quizzes
 - Start at 1100AM...drop lowest score
- Grade
 - (UG) = $0.5(\text{final}) + 0.4(\text{best midterm}) + 0.1(\text{quiz})$
 - (Grad) = $0.1(\text{presentation}) + 0.4(\text{best midterm}) + 0.4(\text{Final}) + 0.1(\text{Quiz})$
- Teaching assistant: Mr. Wontae Joo
 - See the syllabus for office hours



Course Information

- Note the dates of the exams. If you miss an exam that will be your dropped score. There is really no way to make up these exams.
- Students with disabilities may request appropriate academic accommodations from the Division of Diversity and Community Engagement, Services for Students with Disabilities, 512-471-6259, <http://diversity.utexas.edu/disability/>
- Occupants of buildings on The University of Texas at Austin campus are required to evacuate buildings when a fire alarm is activated. Alarm activation or announcement requires exiting and assembling outside and across the bridge to assemble between ECJ and RLM.
 - Familiarize yourself with all exit doors of each classroom and building you may occupy. Remember that the nearest exit door may not be the one you used when entering the building.
 - Students requiring assistance in evacuation shall inform their instructor in writing during the first week of class.
 - Do not re-enter a building unless given instructions by the following: Austin Fire Department, The University of Texas at Austin Police Department, or Fire Prevention Services office.

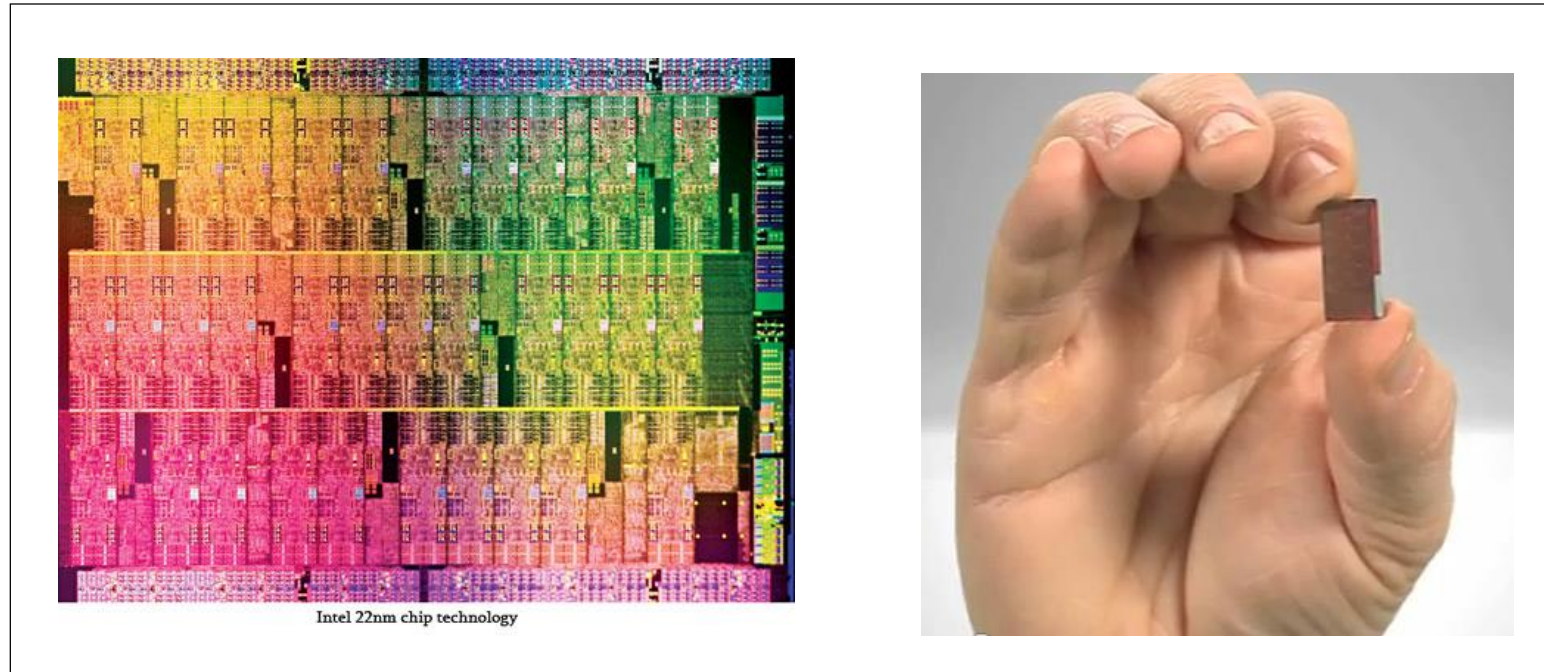


Evacuation Route



Integrated Circuits Today

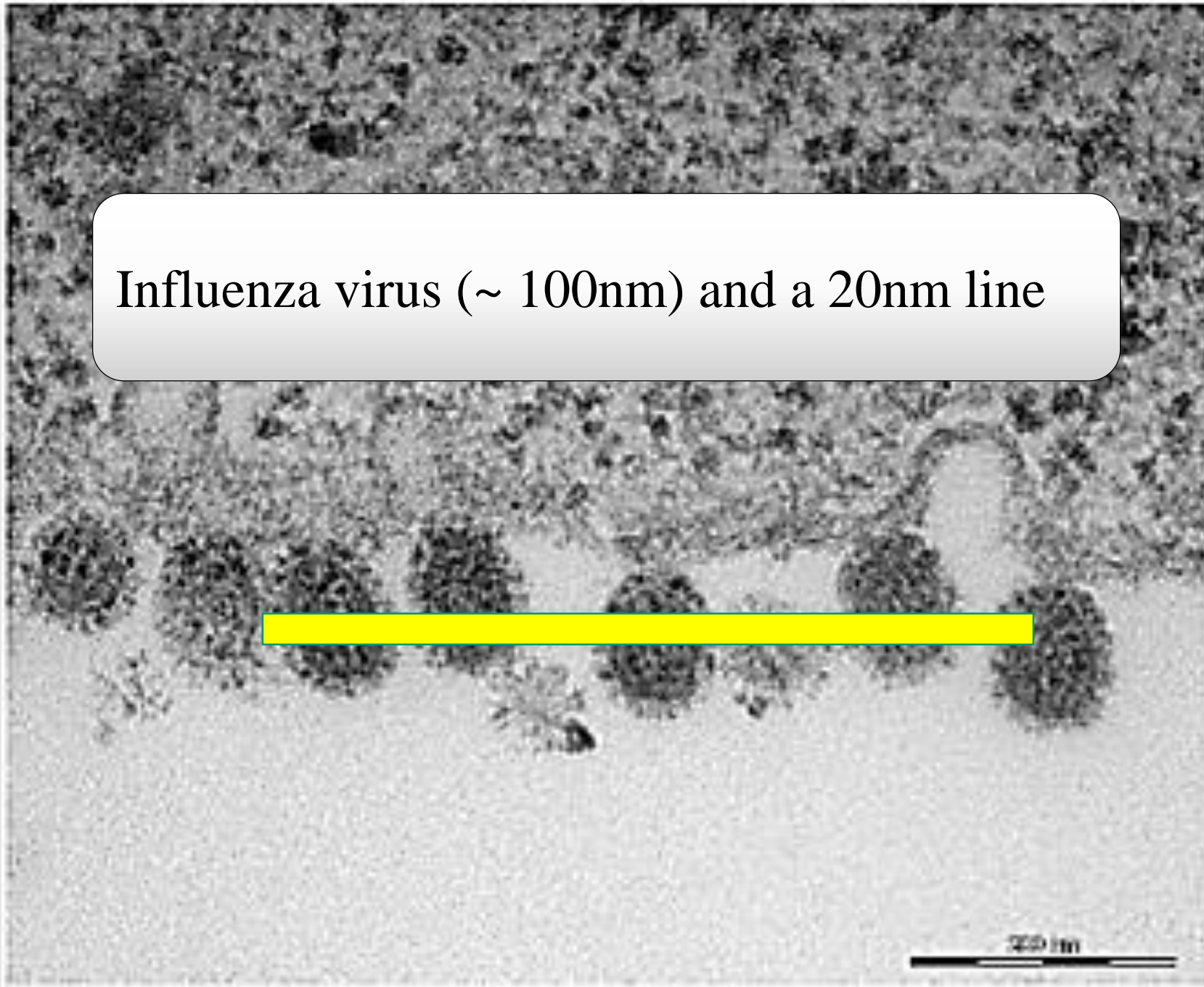
1.4 Billion Transistors



- Intel microprocessor with **22 nm** minimum features
 - Features are smaller than a virus!
- One of these transistors costs less than one printed character in the Austin American Statesman!



Influenza virus (~ 100nm) and a 20nm line



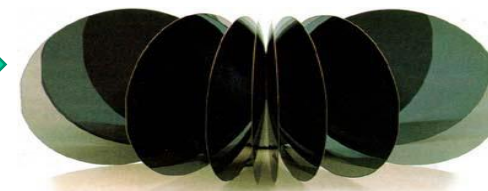
We will discuss the materials and processes used to make these tiny structures



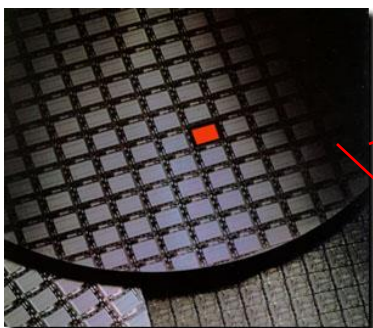
sand



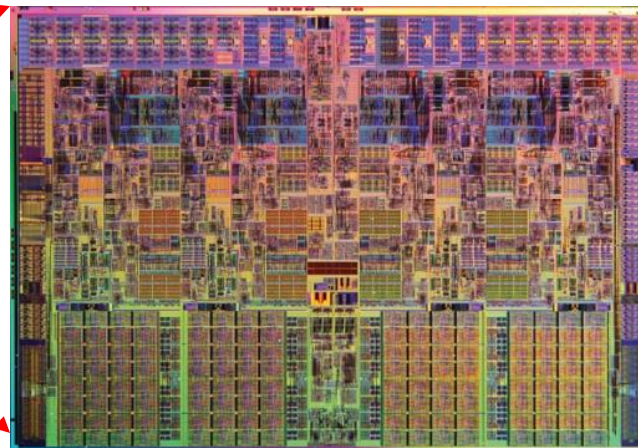
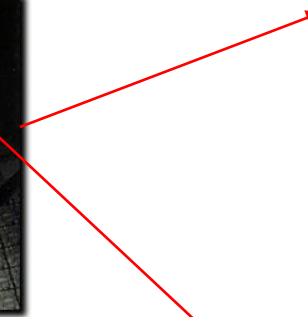
Single crystal Si Ingot



Polished Si Wafers



Device Wafer



“Chip”

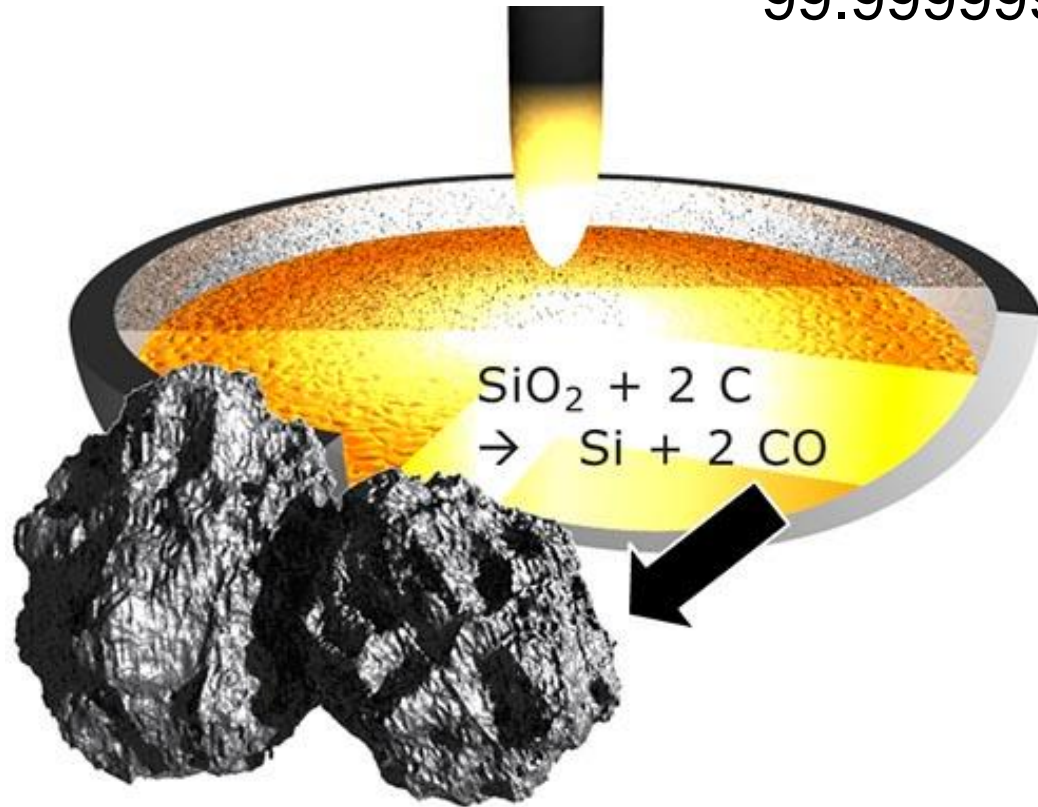


Packaged devices

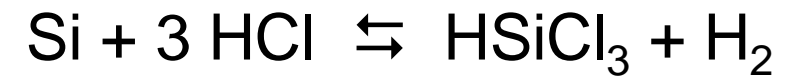


SiO₂ to Poly Silicon

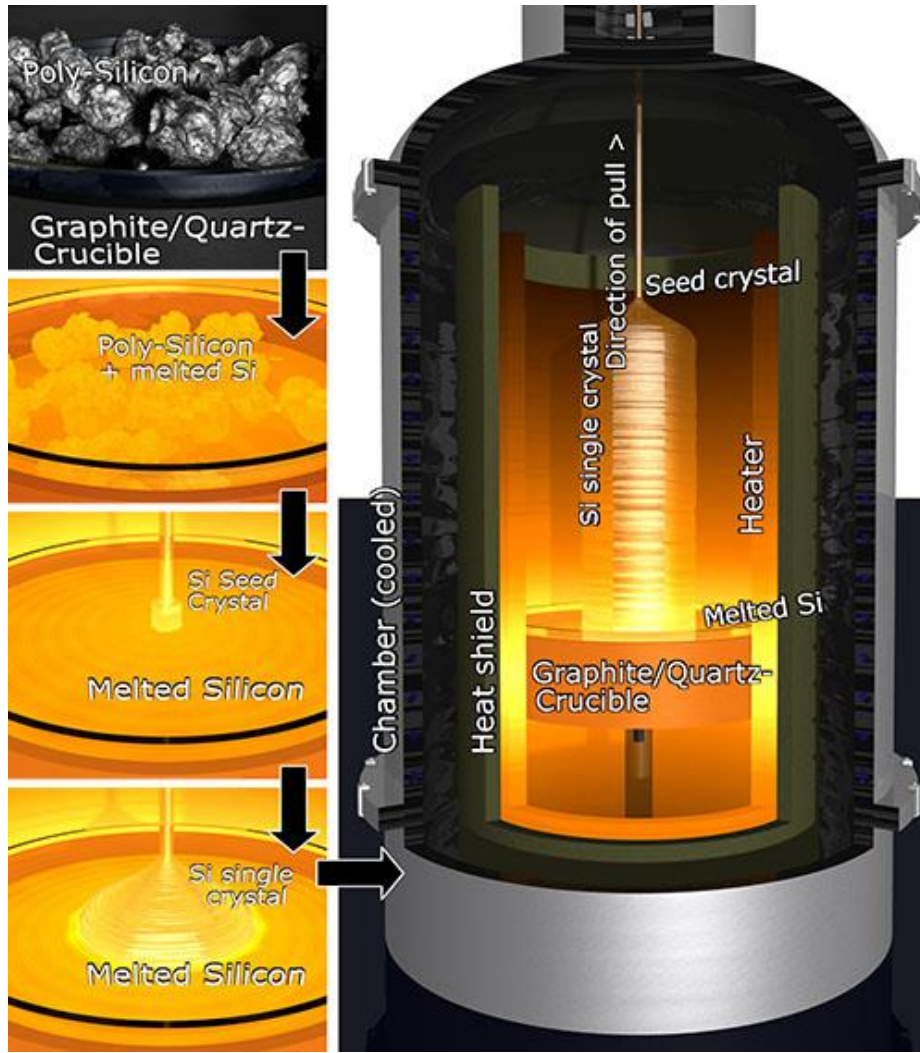
Purification as HSiCl₃ produces
99.9999999% purity



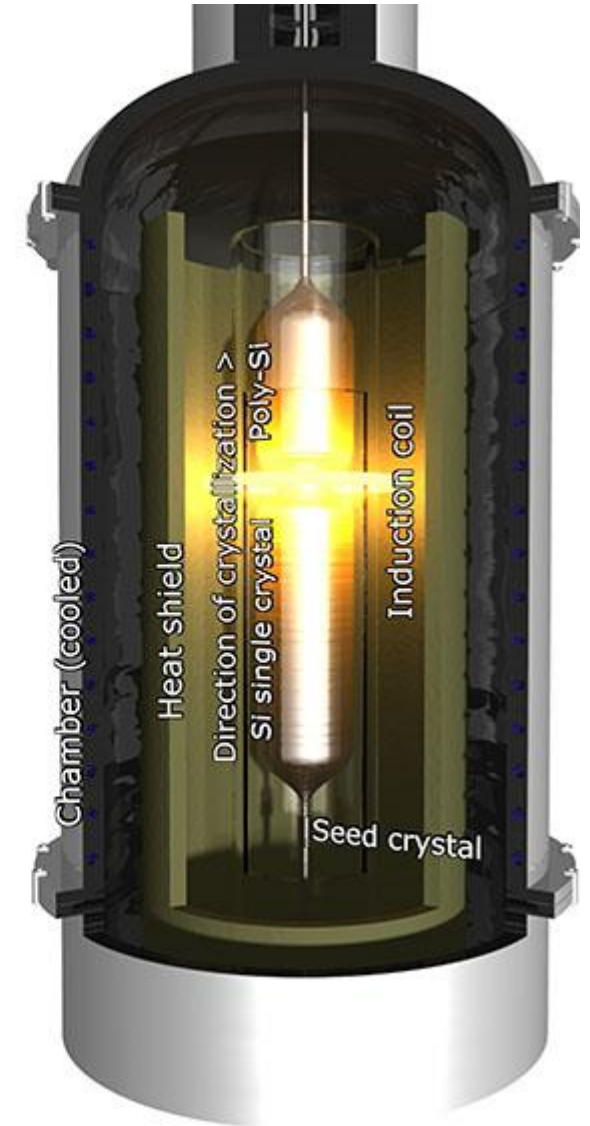
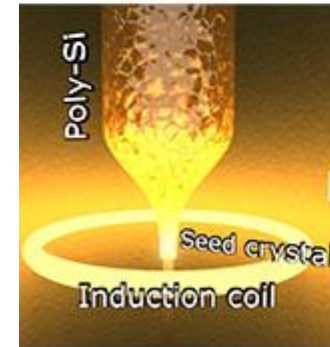
Reduction with Carbon



Silicon Crystal Growth

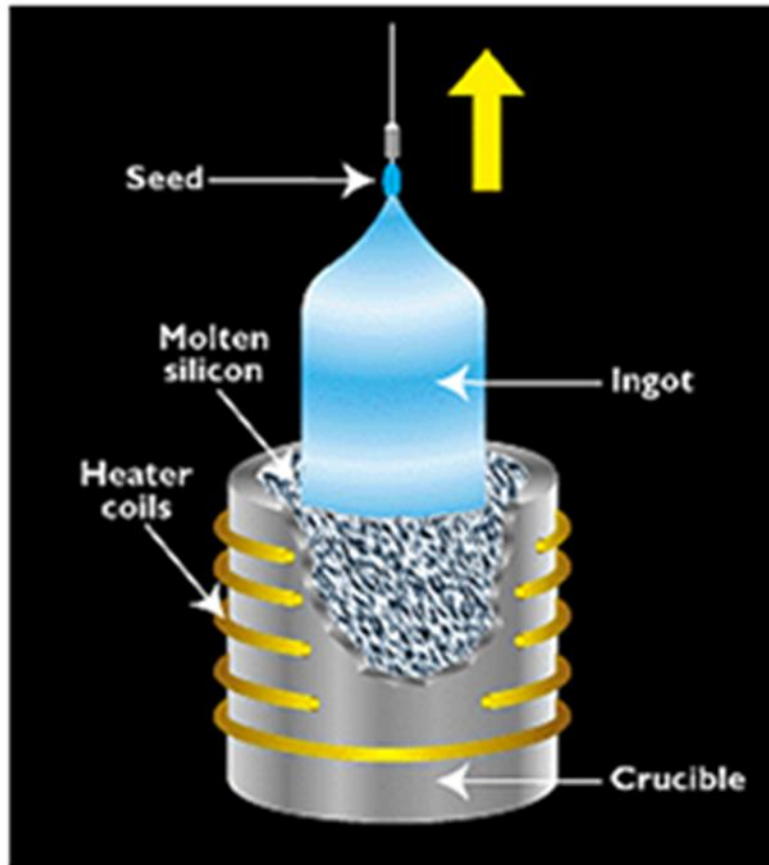
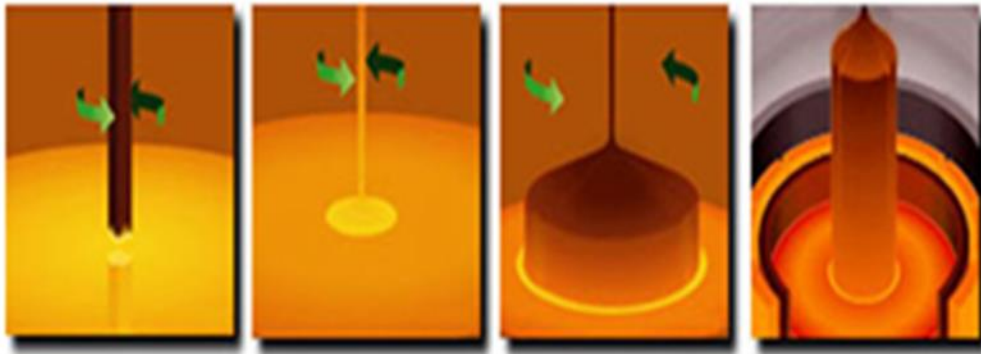


Czochralski-Technique:

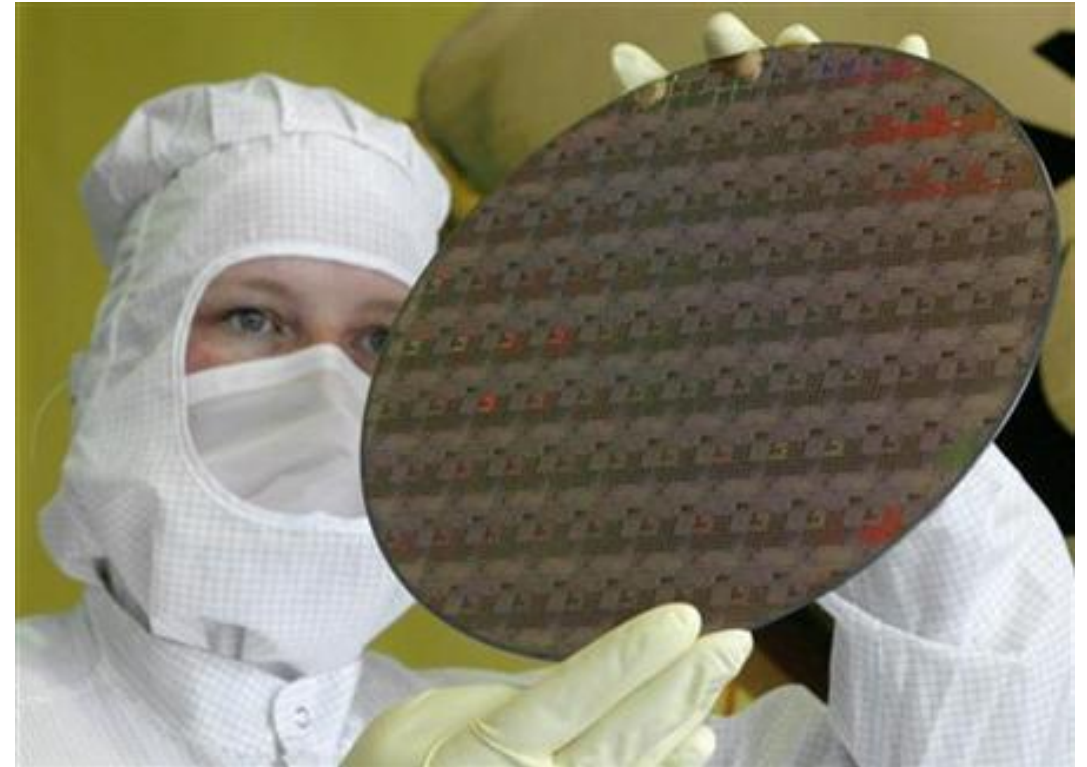
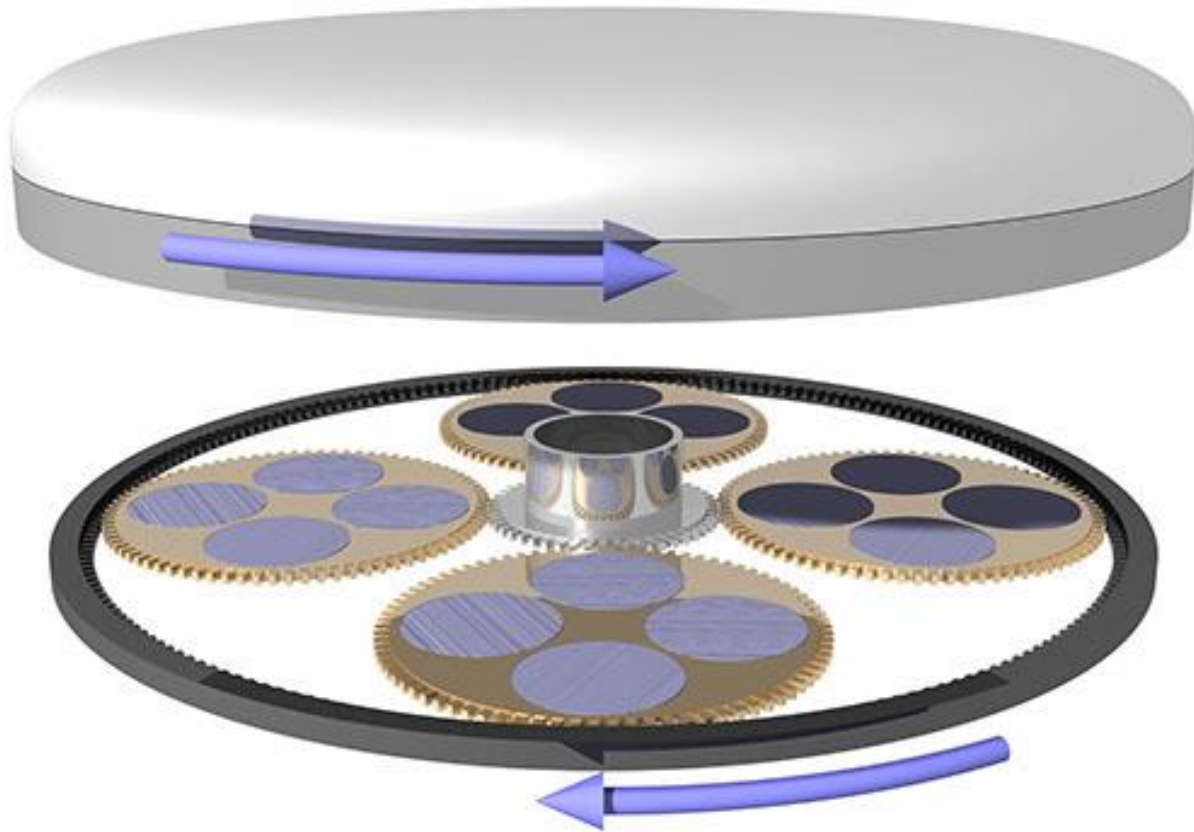


Float-Zone Technique:





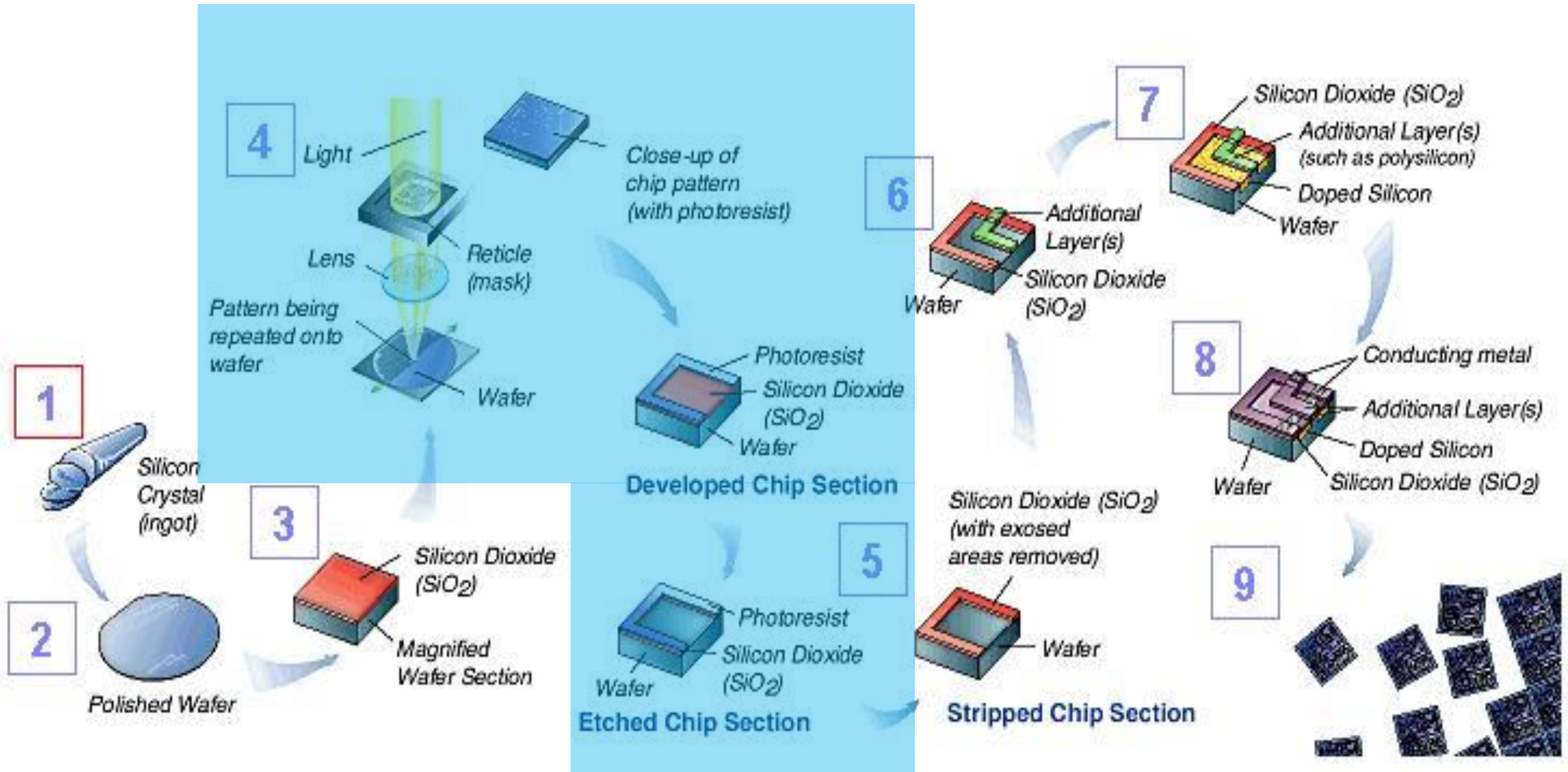
Lapping to Smooth the Wafer



450 mm Wafer

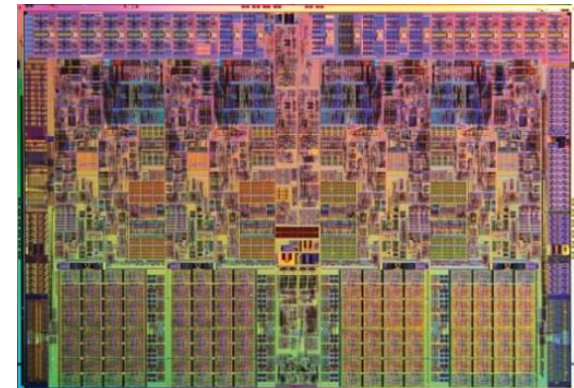
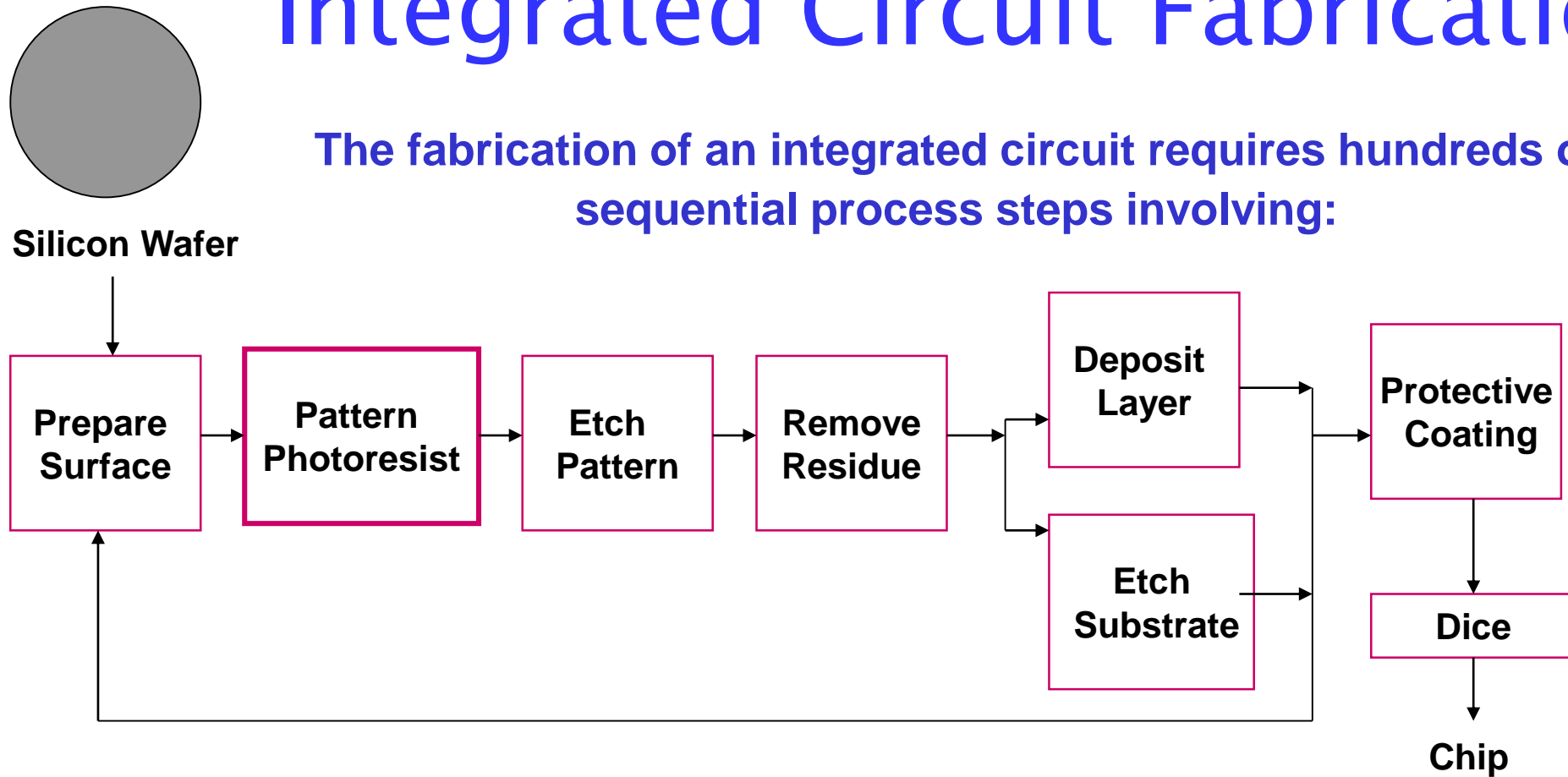


~400 Unit Processes are required

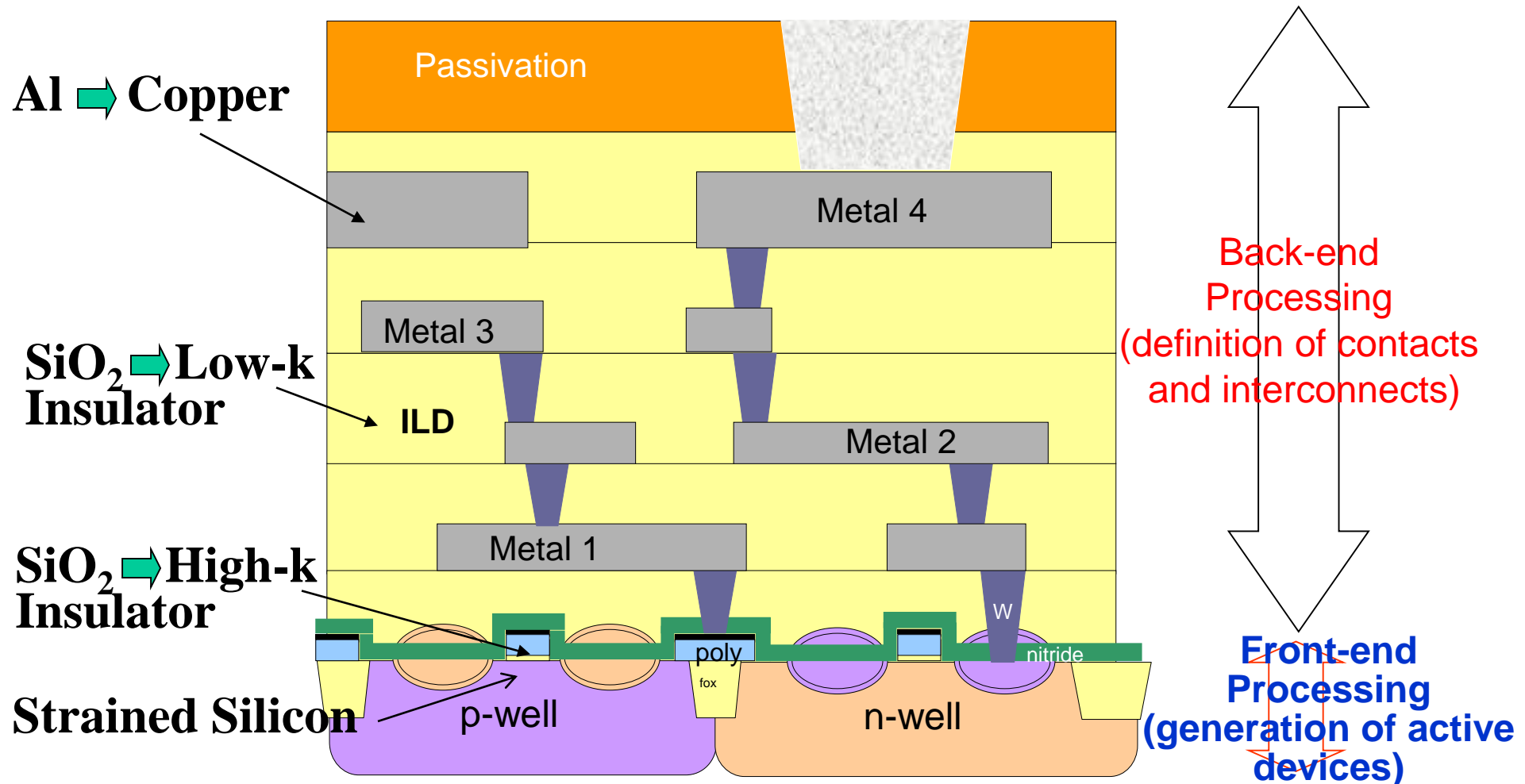


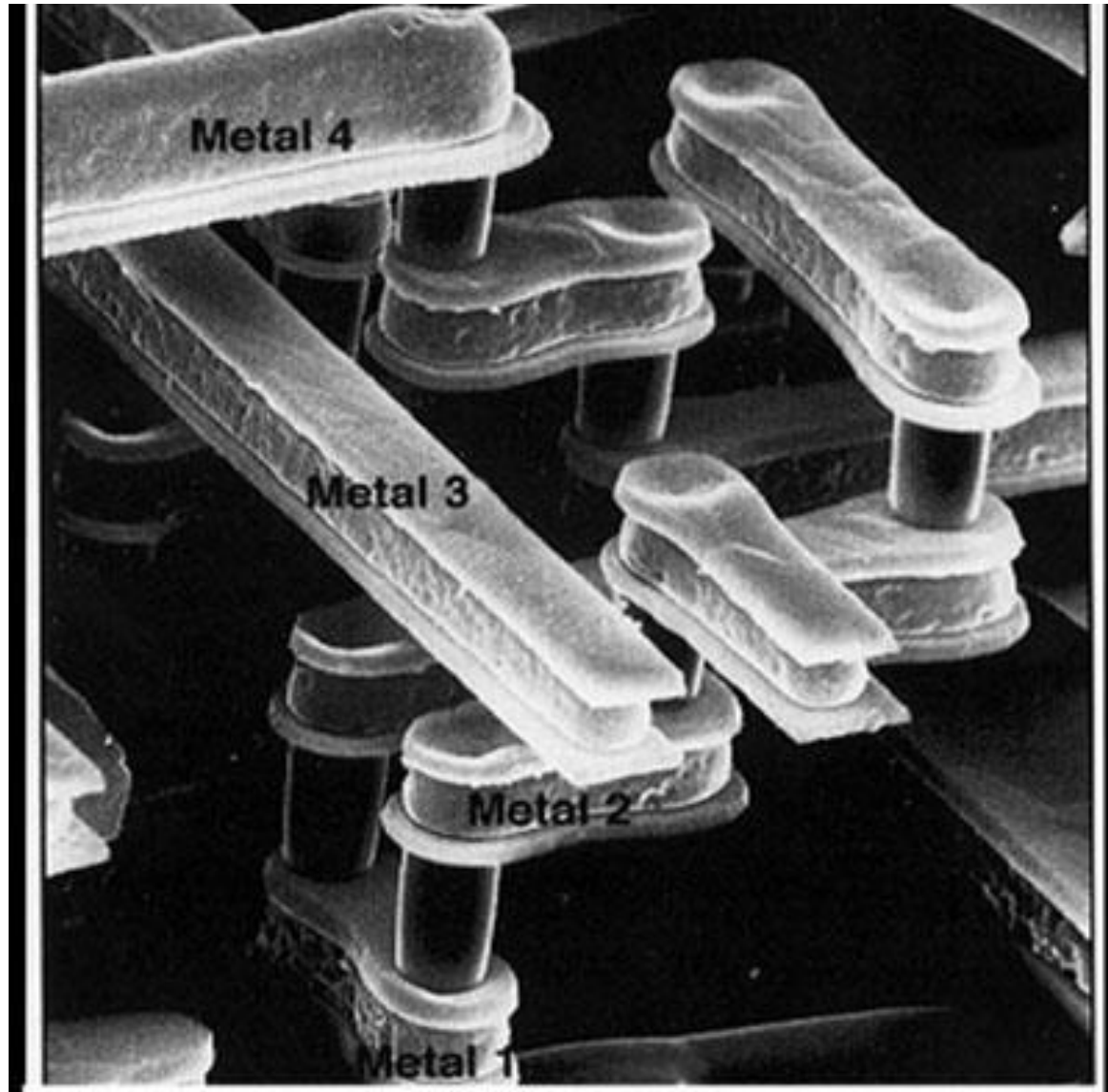
Integrated Circuit Fabrication

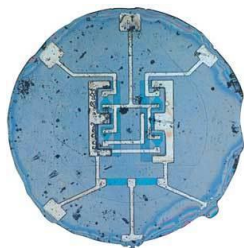
The fabrication of an integrated circuit requires hundreds of sequential process steps involving:



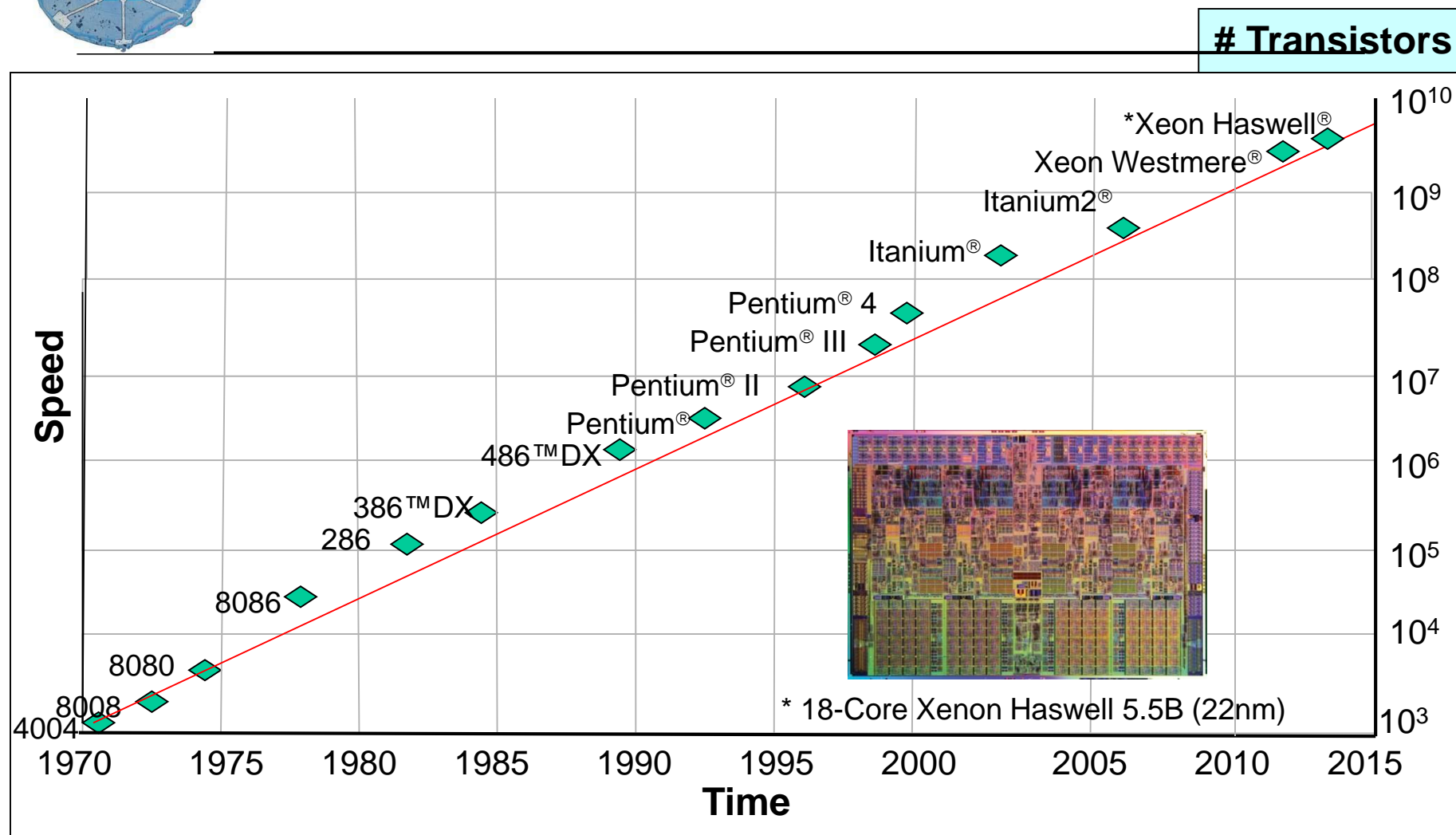
Chip Schematic







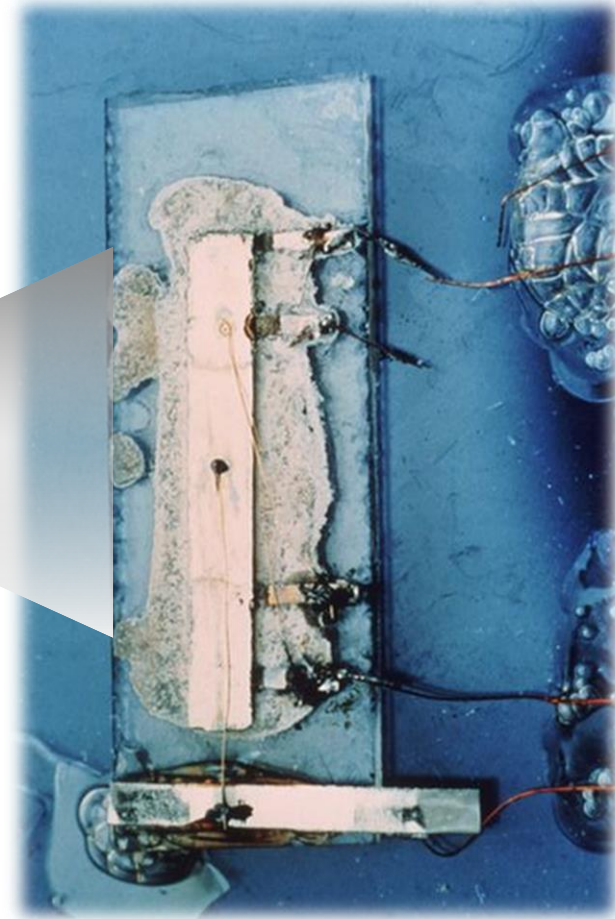
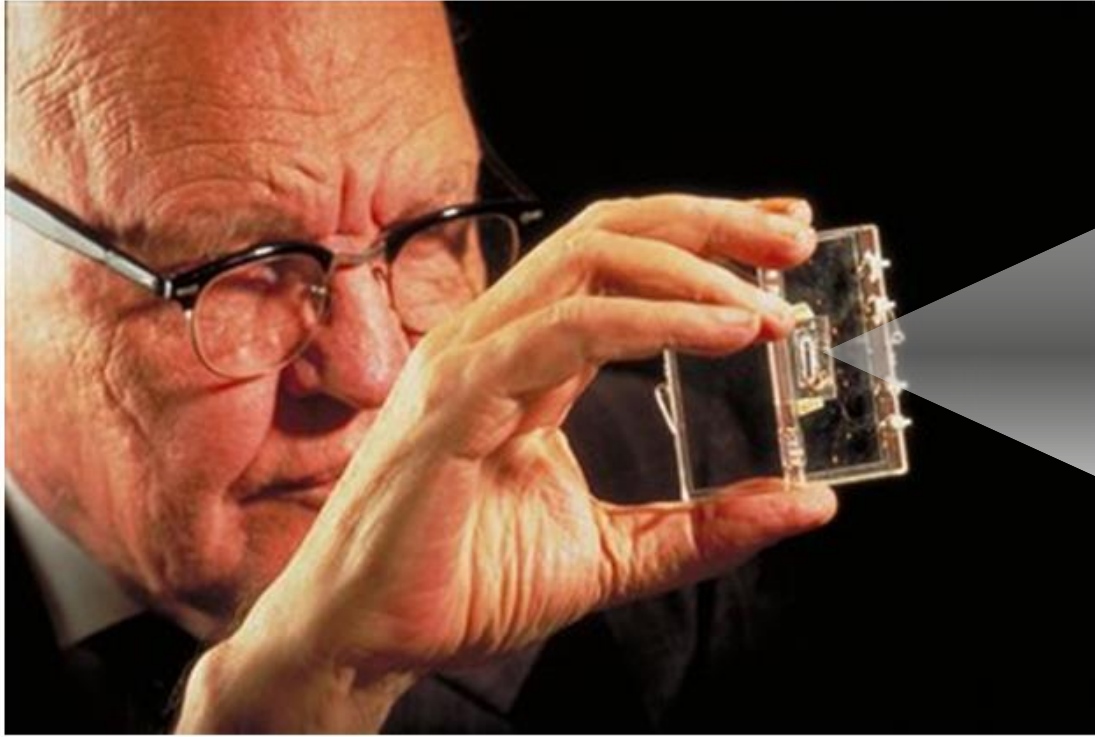
Microprocessor Evolution



Intel claims that by 2026 processors will have as many transistors as there are neurons in a brain



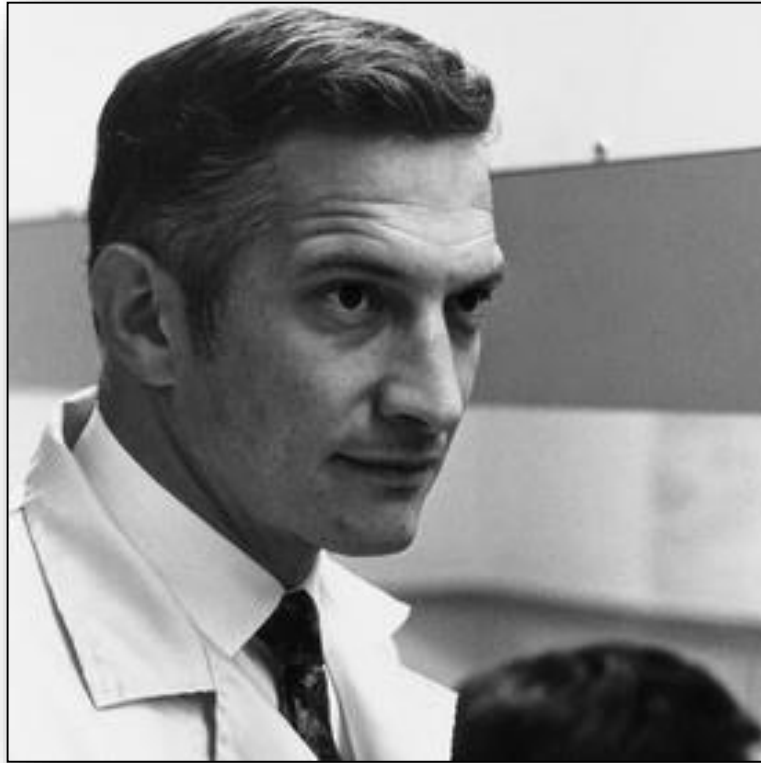
First Integrated Circuit



Jack Noyce with the first
Jack Kilby with the first integrated circuit - 1958
Nobel Prize 2000



Founders of Intel Corp 1968



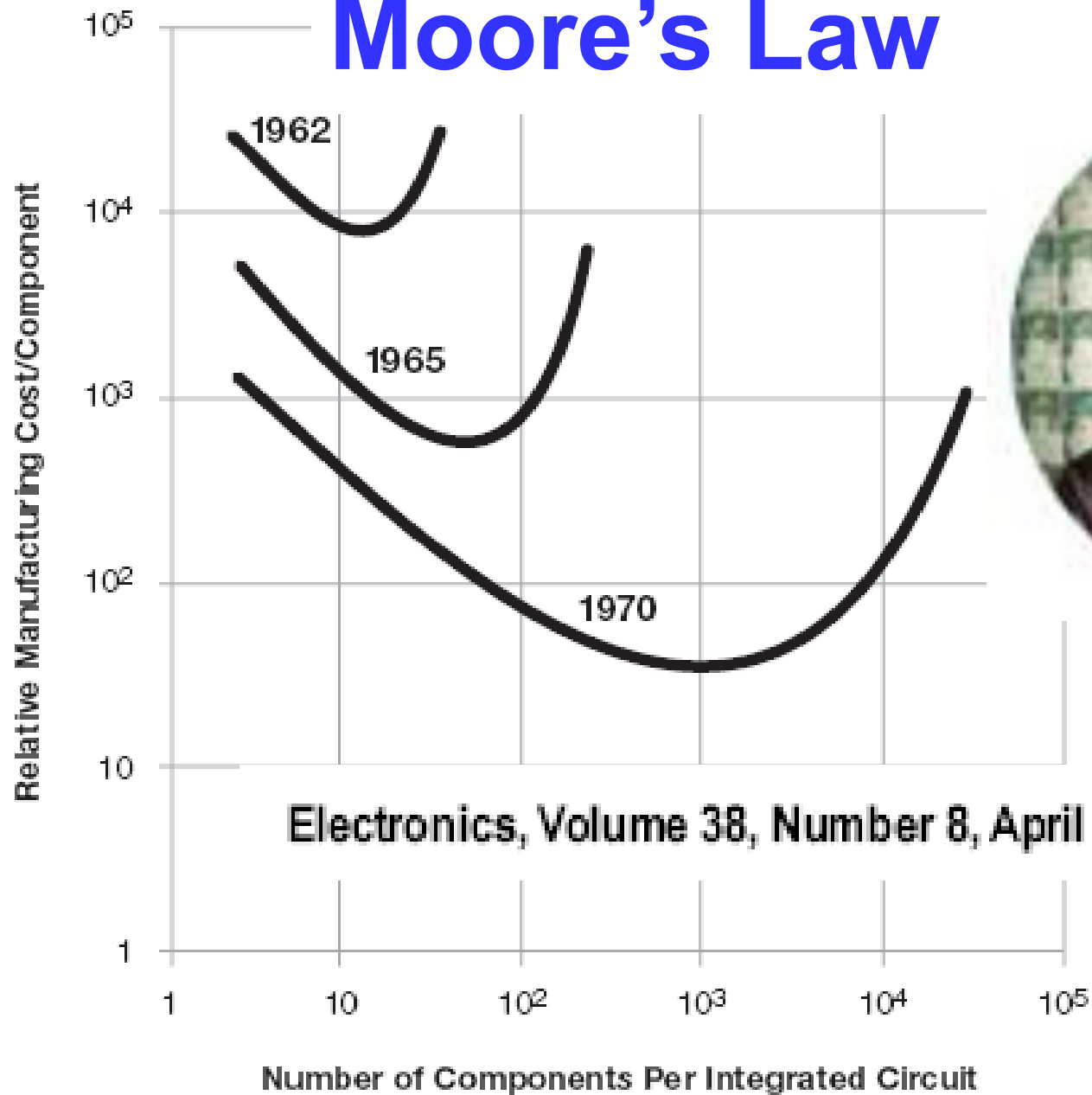
Robert Noyce



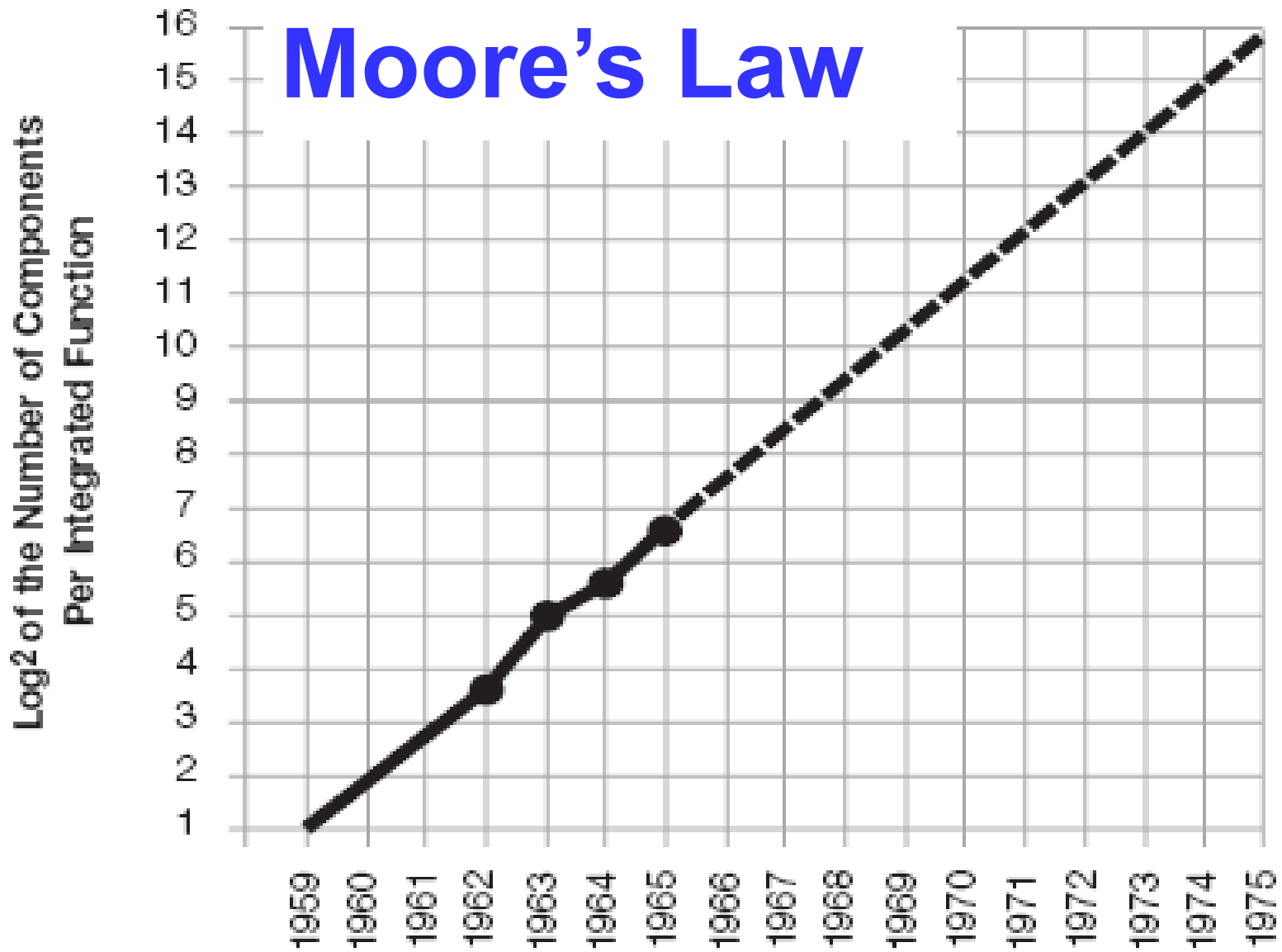
Gordon Moore



Moore's Law



Moore's Law

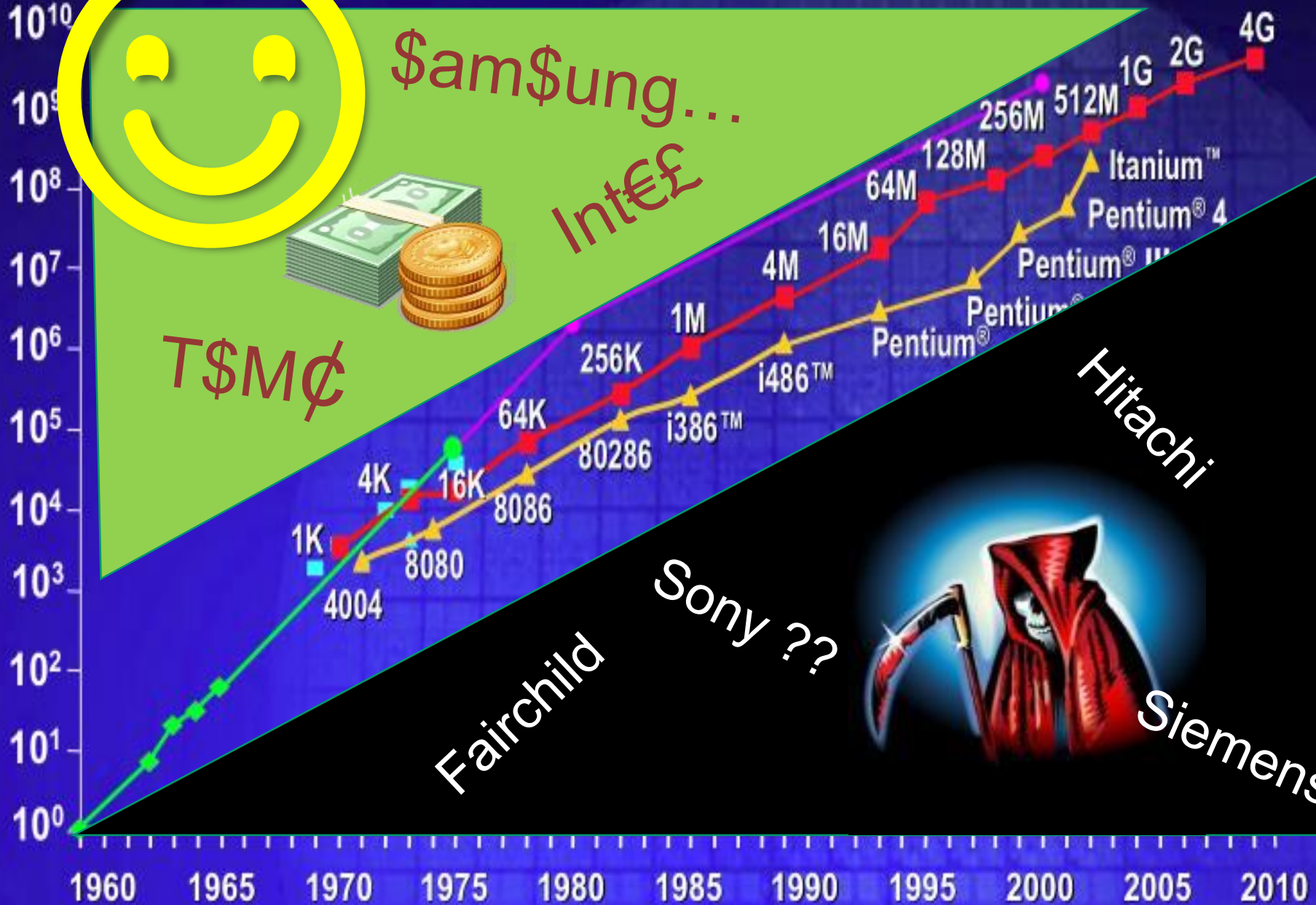


Electronics, Volume 38, Number 8, April 19, 1965



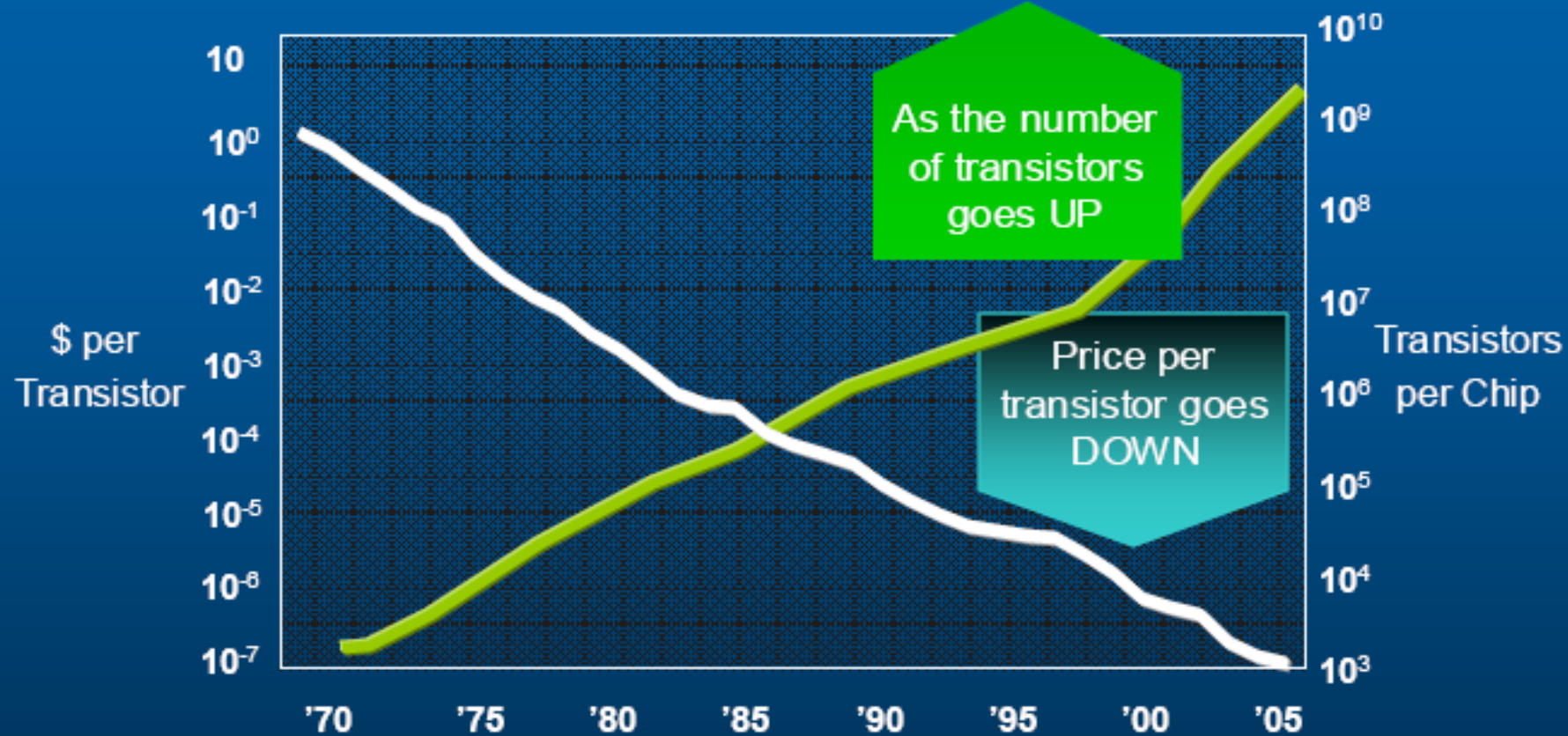
Moore's Law

Transistors
Per Die



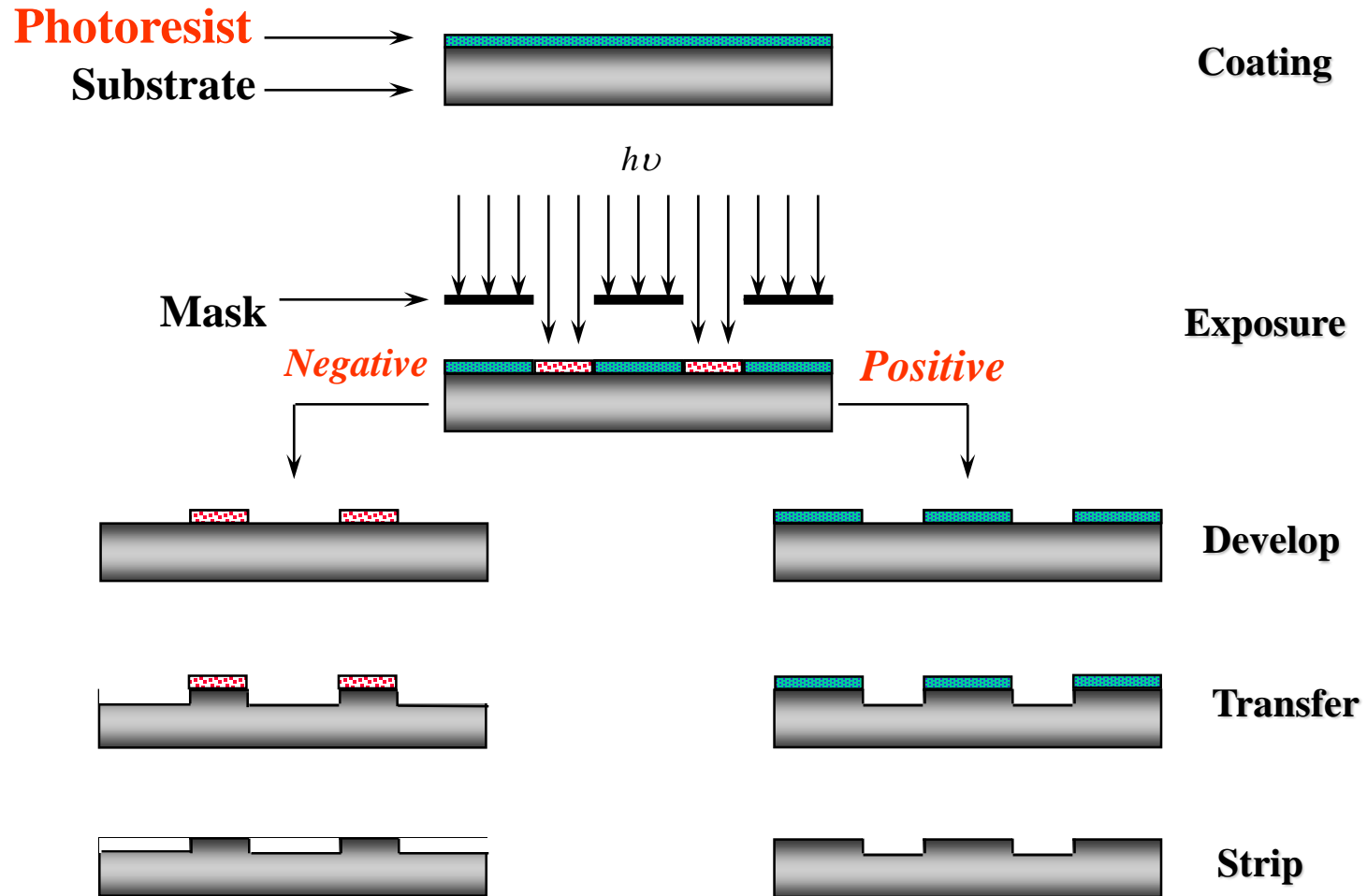
The Driving Force for Progress is \$\$\$

Economics of Moore's Law



Source: WSTS/Dataquest/Intel

Photolithographic Process

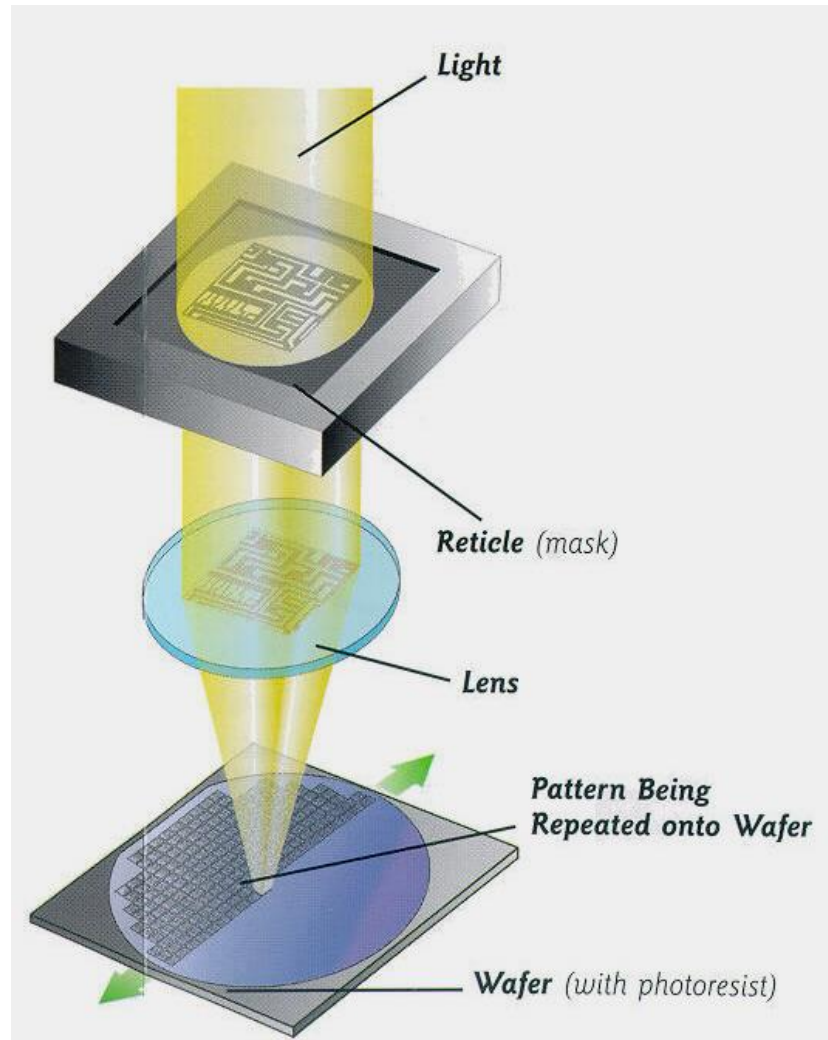


Photoresist



Exposure Systems

$$R = k \frac{\lambda}{NA}$$



Printing tools / Aligners



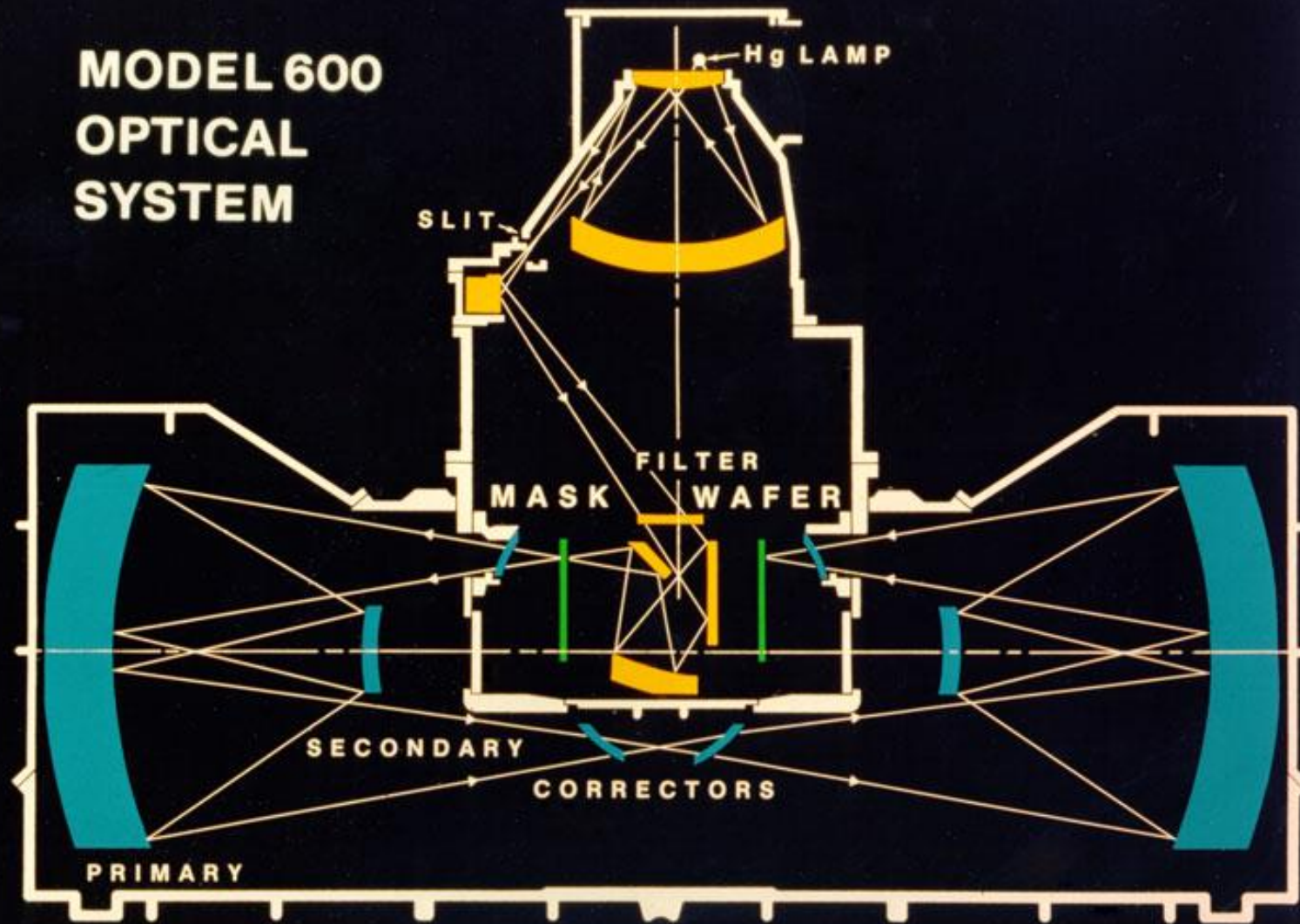
Contact Aligner



Projection Printer



MODEL 600 OPTICAL SYSTEM



U.S. AND FOREIGN PATENTS PENDING



State of the art, 193 nm immersion tool

